Low Power Circuit Design For Footed Quasi Resistance Scheme In 45nm Vlsi Technology-Review

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ABSTRACT

This paper provides detailed information about earlier research works focused on designing and implementing VLSI circuits in terms of power consumption and leakage reduction through various CMOS based methods. A few existing exploration works were centered on diminishing the power spillage in CMOS circuits. Some of them are offered here to comprehend the issues confronted and the fitting arrangements required. Most of the existing methods are developed based on the Domino logic. But, Addition of static inverter is used in the domino logic circuit to eliminate the logic 1 (in precharge phase) to logic 0 (in evaluation phase) transition. This elimination of transition from logic 1 to logic 0 signifies that additional charging and discharging is performed at the output capacitance of static inverter when it is in precharge phase and meanwhile the output of its subsequent evaluation phase is logic 0, which causes significant power dissipation. Thus this paper conducted the detailed literature survey to overcome this power dissipation problem. This problem is solved through various techniques, whereby the pseudo dynamic buffer (PDB) model significantly reduces power dissipation and hence saves power. However, in the PDB model we have logic 1 (in precharge) to logic 0 (in evaluation) transition which results in faulty output when used for designing of cascaded circuits. Thus, to slove this problem, this survey identified Footed Quasi resistance (FQR) is prominent solution as compared to the PDB model, FQR topology solves the problems caused due to cascading. Moreover, FQR model has lower power dissipation as compared to domino logic model.

I. INTRODUCTION

In current day scenarios, requirement of high battery life becomes mandatory. The gadgets developed with android operating systems dissipate more power when more applications run simultaneously. Reduction in power dissipation and area are the important constraints in VLSI circuits. Integrated circuits are the least expensive devices to make logic gates in large volumes. Integrated circuits usually incorporate the logic gates inside a single chip. Chip design is classified based on the basis of the transistors in the chip.Logic gates form the basis of digital circuits, where as transistors become the basic building block of the logic gates. Digital circuits are implemented using different technologies such as Transistor-Transistor Logic (TTL)[1], Emitter Coupled Logic (ECL)[2] and Complementary Metal oxide Semiconductors (CMOS) [3]. CMOS circuits are considered the best among the different logic families because of their high speed, high circuit density and low power dissipation. In the current scenario, there are many micro devices being developed. This is made possible only with CMOS devices in VLSI. In order to achieve higher speed in CMOS circuits, lower nanometer technologies are opted. In lower nanometer technologies, power dissipation decreases but it increases as speed increases. Hence there exists a tradeoff between speed and

power dissipation. Currently reduction of power dissipation has become mandatory.In distinct styles of standards for designing VLSI circuits, the power optimization is an important one. The processor's design [4] constantly has large challenges in processor structure in which the huge layout denotes the space of various parameters and optimization. In any case, the circuit outline for advancement should recollect a few various factors, for example, the execution and the duration of interconnect twine. In view of the previously stated plan requirements an outline activates with concurrent development. In this unique circumstance, the prevailing evaluates and appears at the streamlining of power factors in software which is mapped with the VLSI design. A few existing exploration works were centered on diminishing the power spillage in CMOS circuits.

Some of them are offered here to comprehend the issues confronted and the fitting arrangements required.Over the past decade, tremendous developments have been seen in the field of CMOS high speed circuit applications. This has been enhanced by the advancements made in the device processing technology as well as the demand from the manufacturing company to integrate them with the digital circuits. As the industry keeps on growing the packing density of the chips, to carry out the Moore's law, it is becoming even harder for the VLSI design engineers to decide the accurate operating frequency of the digital circuits. This is greatly attributed to the variations in the channel resistance, the gate capacitance and finally the propagation delay of the logic gates and flip-flops and finally the digital circuits. The problem with the submicron devices is that the approximation made in case of long channel MOS transistors is not valid. This leads to a variety of effects which are generally overlooked in the long channel length MOS modeling. One of the factors is the difficulty in the scaling of threshold voltage (Vth) which is limited by channel length, temperature, process and drain voltage induced capacitance [6]. In addition, large gate to source voltage (Vgs) induce more electric field between the gate and the channel.This limits the channel area for the charge carriers, which results in increased charge scattering, and therefore mobility decreases [7]. This degradation affects the device transconductance.

Voltage saturation is one of the issues which is important at lower channel length due to higher vertical electric field. This leads to a reduction in the saturation current and weaken the device performance even further. High electric fields due to increasing drain-source voltage also lead to increase the kinetic energy of the carriers, referred to as hot carriers [8]. These carriers account for impact ionization which induces drain-substrate current and at very high fields, even gate current. An additional issue is the Vds dependence of the output resistance (ro).A linear relationship between r0and Vds. But, as the latter increases, impact ionization effect becomes more prominent which increases the drain current, thus reducing r0. This variation leads to nonlinear effects in many circuit applications. The non-regularity of transistor characteristics results timing variations in high speed CMOS circuit applications[9]. It is critical to understand and quantify process induced variability to avoid unnecessarily pessimistic designs. Improving the modeling of both process and environment variables can help designers to decide accurate operating frequency of high speed CMOS circuit.

II. FUNDAMENTALS OF DOMINO LOGIC

Domino logic circuits offer a significant edge over the existing technology due to their faster transitions and glitch-free operation. One of the most effective technologies to implement high speed logic functions is the execution of circuits using Domino Logic. Domino logic [10] is evolved from the dynamic logic technology and is based on the CMOS based implementation of logic function using either PMOS or NMOS transistors. It provides a speed at least twice as faster than the corresponding static CMOS logic. In domino logic, a single clock is used for the process of precharge and evaluation of a cascaded implementation of dynamic logic blocks.The circuit implementation of a logic function is done using 2N devices when Static CMOS logic has a fan-in of N. A range of methods have been provided to decrease the amount of transistors that are needed to perform a particular logic function, including pseudo-NMOS, dynamic logic[11], pass transistor logic etc. There occurs static power dissipation when the functions are implemented using pseudo – NMOS logic since it requires N+1 number of transistors in order to design a

logic gate that has N inputs. An alternative logic type called dynamic logic is described in this report that achieves a comparable outcome while avoiding the usage of static power.
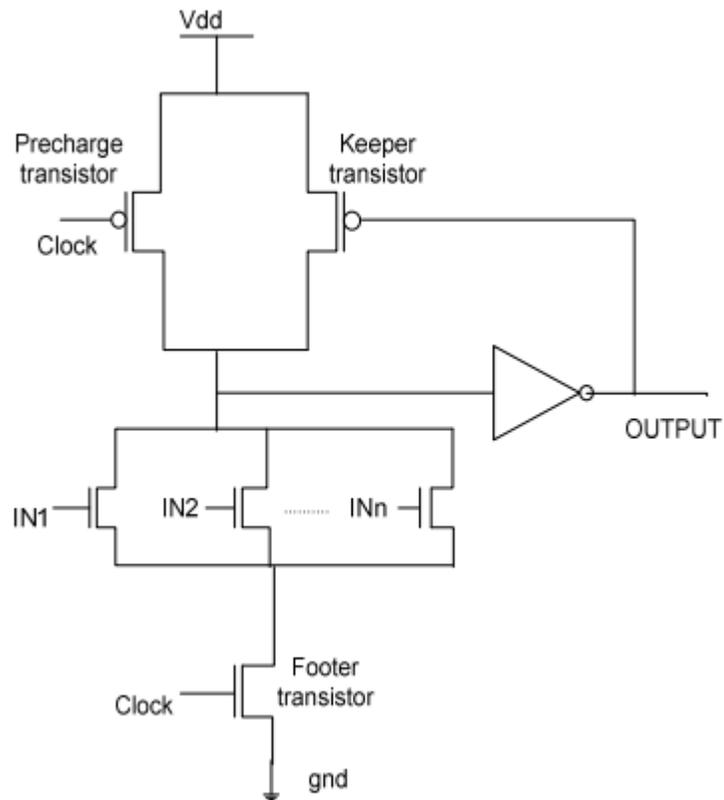

Fig. 1: Footed domino logic

The primary implementation of an N-type dynamic logic gate is depicted in Fig. 1. it can be perceived that the implementation of PDN (pull-down network) [12] is exactly similar to that of the implementation done using CMOS. The operation of n-type dynamic logic gate is divided into two major phases:1) Precharge 2) Evaluation. The mode of operation of the designed circuit is determined by the clock signal (CLK) provided.

Precharge Mode: When the clock input applied to the circuit is 0, i.e., CLK = 0, the PMOS transistor (represented as Mp) precharges the output node (OUT) to a value VDD. Thus, when clock input is 0, the pull-down path is disabled as the evaluate NMOS transistor is switched off. The evaluate transistor eliminates the consumption of static power that occurs during the precharge period. This static power consumption occurs when both the pull-down and pull-up devices are turned on simultaneously and as a result static current flows between the supplies.

Evaluation Mode: When the clock input applied to the circuit is 1, i.e., CLK = 1, the evaluation transistor (Me) is in 'ON' state which implies that it is in operating condition whereas the precharge transistor (Mp) is in switched 'OFF' state. The output value OUT is discharged conditionally which depends upon the input values applied to the logic circuit as well as the 3 pull-down topology. A low resistance path is created between OUT node and GND when the pull-down network (PDN) is conducting which causes the output value to be discharged to 0. However, if the inputs applied are such that the PDN is in conducting state, the value that is contained by the load capacitance (CL) is the value that has been precharged at the earlier state.

During the evaluation mode of operation, GND is the only possible path that exists as a connection between the output node and the supply voltage. As a result, it is not possible to charge the output load capacitance once OUT have been discharged. This can be done only when the subsequent precharge phase takes place. Therefore, the input values applied to the gates can make at most of one transition while in evaluation phase. While in evaluation phase it might happen that when the pull-down network of the logic function is in 'off' state, the output node enters into high impedance state. Consequently, this functionality of the dynamic circuit design is essentially different from the static equivalent of the same logic function in which a low resistance path always exists between the output node and one of the supply voltages.

There are two output levels: Low output level VOL represented by GND and high output level VOH represented by VDD. The Voltage Transfer Characteristics parameters of dynamic logic circuits are extensively different from that of static CMOS logic gates. It is not possible to apply pure static analysis to the dynamic logic gates because in order to be functional dynamic circuits needs a periodic sequence of precharges as well as evaluations.During the evaluation phase, the pull-down network (PDN) of the dynamic inverter becomes active in nature, which occurs in case the input signal applied to the gate exceeds the threshold voltage of the NMOS pull-down transistor. As a result, the values of switching threshold (VM), VIH and VIL of the logic gate are set equal to threshold voltage (Vtn). This translates to a low value for the NML.

The main concern is to design a circuit that has improved performance. This could be achieved by maintaining a high-drive current that can be attained by ensuring that the threshold voltage is proportionately scaled. However, scaling of the threshold voltage leads to a substantial increase in the sub threshold leakage current.

Addition of static inverter is used in the domino logic circuit to eliminate the logic 1 (in precharge phase) to logic 0 (in evaluation phase) transition. This elimination of transition from logic 1 to logic 0 signifies that additional charging and discharging is performed at the output capacitance of static inverter when it is in precharge phase and meanwhile the output of its subsequent evaluation phase is logic 0, which causes significant power dissipation. This problem is solved through various techniques, whereby the pseudodynamic buffer model significantly reduces power dissipation and hence saves power. However, in the PDB model we have logic 1 (in precharge) to logic 0 (in evaluation) transition which results in faulty output when used for designing of cascaded circuits. As compared to the PDB model, FQR topology solves the problems caused due to cascading. Moreover, FQR model has lower power dissipation as compared to domino logic model.

III. FOOTED QUASI RESISTANCE (FQR) MODEL

As the advancement of technologies is at its peak, rising market strain has driven cutting-edge microprocessors to enhance their performance with each passing year. This progress rate is maintained and kept in flow by using micro-architectural methodologies such as dynamic implementation and execution of designs and pipeline. But the usage of these technologies provides decrementing returns, however, in the present fast developing world, it is now more than ever necessary to use faster circuit techniques to further increase performance. As the technology [13] is being scaled down, it leads to the exponential increase in the leakage of evaluation NMOS transistors because of their lower threshold voltage. The major issue that occurs in PDB implementation is the cascading problem at the output node, when the input signal applied makes a transition from logic l to logic 0. Implementing logic functions using FQR technique can overcome this issue. The structure for FQR [14] implementation is as shown in Fig. 2.

In this circuit, the logic function is being designed by using depletion PMOS and NMOS, both of which are being driven by same input node Y. When the node Y is at logic l logic 1, depletion PMOS is OFF thus making quasi resistance acting as open circuit, which is same as in case of logic 0 at node Y but at this time depletion NMOS is OFF which results same. This process can be explained as follows: When the input signal (A) being applied is logic 1, then in precharge mode of operation, the node Y is connected to VDD and in evaluation phase it is connected to ground which makes FQR work as PDB only. When the input

signal (A) being applied is logic 0, the footed quasi resistance functionality in evaluation and precharge phase can be explained as below:
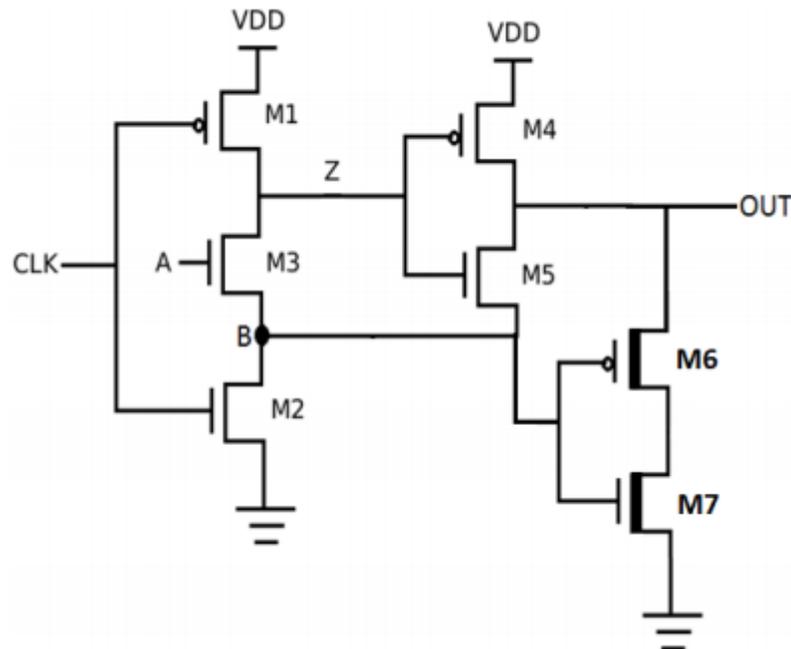

Figure 2: Domino logic circuit using footed quasi resistance

- During precharge phase, both the transistors NM2 and NM5 are in cut-off condition which will lead node Y to act as an open circuit. This happens due to the fact that we are using depletion NMOS and PMOS in FQR which provides a path to discharge the output parasitic capacitance.
- During evaluation phase, both the NMOS transistors, NM2 and NM5 are turned on thus causing the output node to be at voltage 0.

With the enhancement in the electronics industry, domino logic topology is being actively utilized for the designing of enhanced speed and better performance microcontrollers and microprocessors. The usage of domino logic enables to attain the adequate timing objectives. Their improved performance and enhanced efficiency can be attributed to factors such as reduced input capacitance, lower value of switching thresholds and decreased use of logic gates to implement the design. However, a trade-off occurs between power dissipation and speed. As the speed of a design is improved it leads to enhanced power dissipation.

IV. LITERATURE SURVEY

4.1 Studies related to CMOS design and Dynamic Power Management (DPM)

In [14] authors proposed a method for optimizing the yield of design in the occurrence of process variations for estimating the given frequency constraints and power using the mathematical framework. This proposed model was validated by the simulations of monte Carlo SPICE in the process of CMOS as well as proved typical error lower than the 5%. Further, they verified the significance of selected threshold voltage and optimal supply for detaining maximization. The simulation results prove highly sensitive towards supply voltage with 5% variations in supply voltage that is potentially leading towards nearly 15% acquiesce deprivation. However, this study needs improvements towards extending the analysis within die variation.

In [15] authorsdiscussed various methods for device requirement based on the designers. Also they widely studied the size of boost and buck converter of MOS switches. They intended to provide instructions for prospective designers in the area of VLSI and power electronics engineering. Its look forward to focus on all the methods towards resolving difficulties addressed for design CMOS boost and dc-dc buck converter.

However, this study fails to focus on design and verification of optimized converter parameter by the use of VLSI design model.

In [16] authorsproposed a combination of approximate adders for improving the energy efficiency and area of FIR filters implemented in CMOS design. Further, they verified the energy per savings as well as reduction of hardware size in the filters with various method of design. This depends on the various approximation levels within the ripple carry adders that are part of implemented filters in hardware which is fully synthesized in CMOS design as well as related to the accurate execution of the same filter. The simulation results proves the exploration of energy savings that are in the low power optimized circuits by relative computing method. This was validated with reduction of energy and area till 15.5% and 18.8% as correspondingly, except compromising the frequency responses of filters or SNR of recorded as 16-bit audio signals. However, this study needs to focus towards minimizing the energy consumption as well as the area.

In [17] authorsreviewed the power optimization technique which involves the policies and sources. Among the various methods the DPM implies to alter the states while they are not functioning at the high speed otherwise, the full capacity is most effective. This associated the figure that specifies the concept of abstract DPM. This study widely reviewed the stochastic and heuristic policies as well as discussed their usage and disadvantages. However, this study only observed the optimization feature but not the other significant elements like power analysis.

In [18] authorsproposed a method by the combination of dynamic power management and less power optimization (frequency scaling and dynamic voltage) with loop transformations towards reducing the power consumption, at the same time as pleasing the period as well as deadline constraints of the application.

In [19] authorsproposed DPM strategy with machine learning method. They leverage the fact which various strategies that outperforms all the devices and workloads. This method is used to adjust the workload changes as well as assured fast convergence towards the optimized performing strategy for all the workloads. The simulation results prove that this method adapts best to altering devices as well as characteristics workload which achieves an overall performance related to the optimized performing strategy at any point in time. However, they planned to enhance this method for incorporating several low power states as well as frequency scaling or dynamic voltage.

These method simulation results are in the reduction of high system level power (minimum: 28.60%, maximum: 55.45% and average: 42.02%). Furthermore, the simulation results formed through stochastic and deterministic approach for realistic benchmarks on average in 4.125% and 12.07% correspondingly to the optimum solution formed through ILP based method. However, this study fails to consider task graphs with control flow dependencies and variable (best case, average or worst case) task execution times.

4.2 Studies related to power optimization using Transistor Sizing

In [20] authorsdeveloped a fast and efficient low power design method using cell libraries. This optimization routine exploits accurate as well as transistor sizing, efficient statistical power estimation methods and input ordering. A delay model is developed based on the input transition time. An augmented cell library that contains cells that have been designed and sized to give good power and delay tradeoffs is constructed keeping area and input ordering in mind.The low power design method developed in this study has utilized a number of tools that includes the statistical power estimation, transistor sizing, and input ordering. Further, they plan to improve the usefulness of this design method which allows various constraints or encompassing various types of circuits as well as designed with this method

In [21] authors opined that transistor sizing is an efficient method towards the reduction of delay, power in digital as well as analog CMOS design of embedded system. Further, they reviewed the various methods such as geometric programming, genetic and monte Carlo algorithm as well as they related the system performance of the previous work. Also, they discussed the various algorithms towards the reduction of transistor sizing and concluded genetic algorithm is the most efficient as well as leads to best performance circuits in the power consumption case.

In [22] authors proposed the analytical formulation for total power consumption of CMOS design with regards to the size of the transistor that involves the short circuit dissipation and capacitive. Further, they

proved that the CMOS design power consumption that is active area convex function as well as minimizing the objective area which was different than the less power dissipation for the size of the transistor method. Also, they proposed a method for the size of the transistor towards reducing the power consumption of CMOS design circuit that is subject to the provided delay constraint. However, this study does not focus on the effect of variation in the supply voltage as well as feature size as a minimum. Essential focus is also towards the study of the transistor sizing issue with feature size and scaling of voltage.

4.3 Studies related to power optimization using clock gating and power gating

In [23] authors proposed an ADL based optimization of low power design that has low complexity as well as capable of various prominent that provides highlevel architectural information. The overall power consumption improved up to 41% in this case study. The simulation results show improved results than the RTL based industrial clock gating method. Further in future, they planned to discover the isolation of ADL based operand method as well as the interface of clock gating inclusion with operand isolation. It involves the decisive effect of clock gating method based on ADL method on the synthesis of clock tree as well as guiding it with directives as high level.

In [24] authors proposed the clock gating method for optimizing the power of programmable Embedded Controller that employs the RISC architecture. Thus the designed CPU supports the on-chip clocking, I/O port, a smart instruction that provides the range of frequencies, controller, and RISC architecture. Thus the overall design was captured by VHDL programming and implemented on FPGA chip design using Xilinx. The combined clock gating with architecture method was found to reduce the power consumption through total power consumption by 33.33% through this chip design.

In [25] authors discussed various methods towards clock gating approach. They found nor based clock gating method has output correctness issues owing to glitches as well as exposure while removing the nor or latch based hazard issues. However, the glitches issues still exist and only a few advanced techniques are devoid of this problem as it is thought to have better power saving method.

In [26] authors proposed a clock gating method for reduction of power and incorporated the different points in the distribution of clock network. Further, they executed the clock gate that is based on AND gate for 3-bit full adder system. The simulation results show the clock power was reduced to 50% based on the clock activity and architecture.

In [27] authors proposed a method for voltage selection and size of the gate which was related to the nonlinear programming for power optimization. For the delayed assignment, they used a level gate based heuristics method that disassociates the delay at each path towards individual gate level as well as optimizing all gates separately for power with its delay constraint. Subsequently, the optimization was achieved at the various gate level, when maintaining the accuracy. The simulation results show the efficiency of this method using ISCAS benchmarks. However, this study needs to examine other optimization issues in the design of VLSI automation.

In [28] authors analyzed the circuits in digital by various types of the power gated circuits with VLSI design method that was based on low power. The nanometer technology produced the various results for various power gating circuits. Further, they demonstrated as well as simulated microwind design.

In [29] authors proposed a power gated sleep technique for designing a circuit. This method produces the minimum speed power product between various technologies. The simulation shows the low leakage power reduction with less speed; particularly it shows the authority than existing method as 50-60%. Further, it will be used as future integrated circuits for the efficiency of power and area.

In [30] authors provided the detailed explanation of the power consumption, dissipation in the operation of CMOS transistors as well as also examining the fundamental mechanisms for power reduction. Resistance induces voltage difference - Maximum IR drop goes down from 1.40% to 1.01%. In future, they planned to extend by adding MultiVt technique along with the coarse grain to analyze how leakage power can be reduced efficiently.

4.4 Studies related to sleep transistor

These rest transistors kill the circuit by removing the power rails. The rest method however turned out to be superior to double Vt and MTCMOS system couldn't give a fantastic bring about diminishing the spillage control. This prompted the creators to plan another better circuit and in this race they proposed another

strategy called the stack procedure which powers a stack impact by separating a current transistor into two half size transistors.

In [31] authors planned to show the examination of spillage segments, extensive investigation and investigation of spillage segments and to display diverse proposed spillage control lessening methods.Power gating method utilizes high Vt PMOS sleep transistors and it cuts off VDD from a circuit piece. The low Vt NMOS rest transistor estimation is an imperative plan parameter. This strategy is otherwise called MTCMOS or Multi-Threshold CMOS. MTCMOS circuit system is broadly embraced for upgraded vitality productivity in elite incorporated circuits.

In this cutting edge world, because of headway of battery-based gadgets with restricted power abilities, real necessity of energy proficiency and power-postpone item is needed. It is fundamental and imperative to evaluate and improve the power utilized as a part of the CMOS based circuit plan. In [32] authors presented that one of the principles behind mind boggling issues in planning inserted frameworks like portable processing, web based handheld gadgets, and specialized gadgets are power estimation and power enhancement.

In [33] authors proposed a philosophy towards evaluating and also enhanced the parametric yield of outline in the event of variety process. Be that as it may, they didn't concentrate on confirmation and also an outline of advancement converter parameters by the plan of VLSI stage. Additionally, the requirements are accentuation towards lessening the area and vitality utilization.

In [34] authors introduced a far-reaching concentrate with a dissected report for different spillage control diminishment procedures. The dissected outcomes demonstrate that the sluggish manager strategy spares a normal of 56% of energy.

In [35] authors tended to the spillage control issue that happened in the 100nm channel gadgets. To give an answer, a circuit technique is displayed where it moderated the spillage control in MOSFET by controlling the voltage in the source terminal and it gets a better arrangement in sparing the power and lessening the power dissemination

In [36] authors expressed and displayed different strategies utilized for limiting the power spillage like Forced Stack, Sleepy Stack and Sleep Transistor. From the execution of these techniques, it is concluded that a standard power spillage decrease strategy is the best technique which is designed by microwind programming.

In [37] authors gave a point by point report which states about different strategies utilized for power spillage decrease in CMOS circuits. After expressing about different strategies, concentrated on a novel strategy called as Scan Chain technique for power spillage lessening and power advancement in CMOS circuits.

In [38] authors proposed a hypothetical approach of energy estimation, control utilization, control advancement and diminishing the power spillage in VLSI circuits. This hypothetical approach concentrated on using low power circuit traverses inside an extensive variety of gadgets in calculation level to the process level.

4.5 Studies related to LECTOR configuration

In [39] authors have proposed an energy efficient adder circuit using two-phase clocked adiabatic logic. Simulation of the 1-bit full adder implemented with the proposed technique gives less power dissipation at lower frequency ranges. The results are compared with TwoPhase Adiabatic Static Clocked Logic, standard CMOS and Positive Feedback Adiabatic Logic. The proposed technique shows a power saving of about 70% when compared to that of CMOS logic. The power consumption of the circuits were analyzed using 0.35 nanometer technology in Pspice.

In [40] authors have proposed use of adiabatic logic for power reduction in CMOS circuits. In this proposed method, energy at the load capacitance can reused rather than wasting as heat dissipation. As adiabatic circuit depends on parameter variations, these are taken in to account for the analysis and the results are compared with efficient charge recovery logic (ECRL) and Positive feedback adiabatic logic (PFAL) for NAND, NOR circuits.

In [41] authors have developed an energy efficient logic which combines both adiabatic logic and non adiabatic modes. Power clock with single phases have been used and this serves as the input to clock

generator. This clock generator converts the single phase clock to an alternating current power clock supply. The results of this are compared with non adiabatic operations. The circuit performance of inverters coined up together is used for comparison. Thus conventional adiabatic logic is implemented in this paper.

In [42] authors designed adiabatic split level charge recovery logic for low power digital VLSI circuit. When compared to static CMOS circuit, split level charge recovery logic has smaller power dissipation. In conventional circuits, bits are thrown for every output transformation, leading to conversion of their energy as heat. This increases the system overhead required to overcome the heat which in turn affects the cost , system weight, short battery life etc. Simulation of a CMOS inverter, a 4 bit carry look ahead adder and a two input NAND gate proved that split level charge recovery logic is power efficient.

In [43] authors described new low power solutions for VLSI circuits. A positive feedback adiabatic logic in which power is reduced by energy recovery during the recovery phase is described in this paper. Energy dissipation comparison with other logic circuits is performed. The results are simulated using Microwind and DSCH. Inverter circuits are taken as a benchmark and to show reduction in power dissipation using PFAL adibabatic circuit.

In [44] authors introduced adiabatic logic families of a second order 2N-2P and 2N-2N2P without using any diode. Over the data valid time, these circuits provide a non-floating output level, whereas the output levels are floating for most adiabatic circuits. These circuits also facilitate excellent power saving without affecting the complexity or size of the circuit when compared to diode based adiabatic logic families. Simulations of these circuits show an expected behavior with respect to adiabatic charging. Also energy saved in these second order adiabatic computing circuits is about $O(Vdd/Vt 2)$ when compared to a conventional static CMOS circuit.

In [45] authors presented the design of a low power multiplier by Asynchronous Adiabatic Logic using Complementary Pass transistor. This multiplier possesses the advantages of both adiabatic logic and asynchronous systems. This design is evaluated with 4, 8 and 16 bit multipliers and the result is compared with Conventional CMOS Logic Design. Investigations show that on comparison with Conventional CMOS Design, the asynchronous adiabatic multiplier circuit has energy saving of about 50% to 74% when operated between the frequency range 100MHz to 300MHz.

In [46] authors proposed adiabatic techniques for building logic gates with less power dissipation. A new CMOS logic was described by the combination of adiabatic theory and CMOS dynamic logic which is referred as the adiabatic dynamic logic. The simple adiabatic dynamic gates can be cascaded and offers low power consumption when compared to that of a conventional CMOS circuit.

In [47] authors designed a one bit hybrid full adder using CMOS, pass transistor logic and transmission gate for reducing the delay and fasten the process. The energy consumed by the proposed method is also found to be low. The proposed adder is implemented in Cadence in 180nm technology. The delay incurred by the circuit is reported as 14.32ps which is very small when compared to the existing adders. The circuit is constructed with a smaller number of transistors there by providing area optimization

In [48] authors implemented different full adder circuits using standard CMOS, DCVSL, TGA, CPL, 16 transistor, 14 transistor, PTL and 8 transistor. Simulation was carried out using Tanner EDA. Propagation delay and power delay product have been compared for different full adder circuits through variation in the supply voltage.

In [49] authors proposed an adder which provides the best tradeoff between delay and area. Quantum-dot cellular automata method is used for designing the logic circuits of the adder as it occupies small area. The proposed 64 bit adder occupies an area of 18.72 μm 2 and provides a delay of 9 clock cycles.

In [50] authors proposed a simple and efficient Carry Select Adder (CSLA) architecture by making gate level modification. This minimizes the power and area of the Carry Select Adder by reducing the number of gates. This modification is extended to 8, 16, 32 and 64 bit square root Carry Select Adder. A comparison of these architectures with the regular square root Carry Select Adder shows reduction in power and area in the proposed work by 15.4% and 17.4% respectively with a slight increase in the delay by 3.76%. It is concluded that the proposed CSLA architecture is low power, low area and is better than the regular square root Carry Select Adder.

In [51] authors presented two designs for a single bit full adder using three transistor XOR gates. AN adder with twelve transistors and an adder with reverse body bias. The former shows power consumption of 1274 µW with maximum output delay of 0.2049 ns. Power consumption variation and maximum output delay variation is given as [1274 - 141.77] µW & [0.2049 - 0.4167] ns with supply voltage varying from [3.3 - 1.8] V. The latter shows power consumption variations of 30 [1270 - 1067.60] µW with varying NMOS reverse bias from [0.0 to - 2.0] V. Simulations show improvements in power consumption when carried out with different supply voltage and with increased reverse bias applied to the transistor.

In [52] authors have proposed a Vedic multiplier based on sutras. When these sutras are implemented in hardware, they work faster but consume more power. This work modifies the architecture of Vedic multiplier to reduce power. The simulation of Vedic multiplier is done in Verilog HDL and Synopsys compiler is used for synthesizing it. Comparison of the earlier multipliers are made in terms of power, area etc.This multiplier shows good improvements in power and hence can be used for DSP applications.

In [53] authors designed a 16x16 Modified Booth multiplier that can be used for digital signal processing and multimedia systems. The proposed multiplier is capable of multiplying signed as well as unsigned numbers. The multiplier operates at a high speed by using the carry select adder. The Modified Booth multiplier designed with carry select adder and a booth encoder uses a minimal hardware thereby dissipating less power. It also occupies reduced chip area and hence reduces the overall cost of the system.

In [54] authors presented a Vedic multiplier that operates at high speed using the methods based on 16 algorithms in Vedic mathematics. The vertical and cross wire method for multiplication proposed in this work is different from that of normal multiplication. An efficient algorithm for multiplication called Urdhva-Tiryagbhyam enables minimum delay for any type of number. This multiplier is coded using Verilog HDL and synthesized using Xilinx.

4.6 COMPARISON OF VARIOUS METHODS

TECHNIQUE	BENEFITS	DRAWBACKS
Memristor	Memristor, a concatenation of memory resistor, is a two terminal element defined by the relationship between flux and charge Q.	However, resistance cannot go below zero. When the current is stopped, the resistance remains in the value that it had earlier. It means that memristor remembers the current that last flowed through it.
memristor ternary logic gates (MTL)	This purposed method is very promising to be appeared to build high performance ternary computing units as well as other applications such as fuzzy logic.	It requires devices with high tolerance because the devices are switching with changing the input.
CMOS	Design of Low Power 14T SRAM using 45 nm CMOS Technology	Can be improved more for other types of VLSI circuits.
MTCMOS	Here MTCMOS are simulated in different layout techniques show considerable reduction in sub threshold leakage and junction leakage currents by the use of double-finger and four-finger techniques.	This way, using smart layout techniques, noise is increased by the common-mode rejection characteristics of the logic,
DTCMOS	This purposed method is very promising to be appeared to build high performance dynamic threshold computing units.	Because of low threshold voltage and negligible gate oxide thickness, there is considerable increase in the leakage energy consumption.
floating-gate MOS (FGMOS)	It consists of a -channel MOS transistor with a floating gate (first polysilicon layer) over the channel and	This implementation has to be extended further to analyze various performances.

	in some cases extending over to the field oxide area.	
PTL	Pass transistor logic and transmission gate for reducing the delay and fasten the process.	But these dynamic PTL circuits, were also showing some undesirable features such as higher leakage current and less noise immunity which prevent wide utilizing of dynamic circuits.
TGL	Further, they proved that the TGL design power consumption that is active area convex function as well as minimizing the objective area which was different than the less power dissipation for the size of the transistor method.	the size of the transistor increases towards reducing the power consumption of TGL design circuit that is subject to the provided delay constraint.
Heterojunction Tunneling Transistor (HETTs)	HETTs method for device requirement based on the designers. Also they widely studied the size of boost and buck converter of MOS switches.	However, this study fails to focus on design and verification of optimized operational parameter by the use of VLSI design model.
FinFETs	To overcome the disadvantage of larger dynamic power dissipation in No RAce (NORA) logic based dynamic circuits, a keeper has been designed. Considering the aforementioned factors, the objective of this project is to design a keeper for NORA logic based dynamic circuits.	Static power dissipation occurs due to the presence of various leakage currents such as sub threshold leakage, Gate oxide tunneling leakage, etc.
CNFETs	CNT is a type of carbon allotropic which is depended from the fullerenes family. A small nano sized carbon atoms are used to make the CNTs and they are in seamless cylindrical form of mono atomic layered thick grapheme sheet .	But there is no availability of accurate device to perform these ternary or multi-valued logics. So, some new as well as trending technology is required for performing the multi valued logic. But, these are still in early stage of development.
Schottky-barrier CNFET (SB-CNFET)	Power gating method utilizes high Vt PMOS sleep transistors and it cuts off VDD from a circuit piece. The low Vt NMOS rest transistor estimation is an imperative plan parameter.	SB-CNFET circuit system is broadly embraced for upgraded vitality productivity in elite incorporated circuits.
GAAFET	Much improved electrostatic control of the gate can be achieved with the use of gate all around field effect transistor (GAAFET) in which the insulating oxide and the gate electrode wraps around the channel material from all sides.	However, due to downscaling of devices the drain voltage also gets effective in controlling the channel region in addition to gate voltage
Power Gating	Leakage Power Reduction in Deep Submicron VLSI Circuits Using Delay-Based Power Gating"	There is no much drawback apart. This can be improved more to increase other forms of gating.
GDI	it is possible to calculate Convolution of long sequences is very easily. Also,	The designing of a circuit depends upon three major factors namely less power, more

	a GDI technique is used for execution of convolution.	speed and few on chip area for an efficient performance and better marketing of the product
LECTOR	In this proposed method, energy at the load capacitance can reused rather than wasting as heat dissipation.	Because of low threshold voltage and negligible gate oxide thickness, there is considerable increase in the leakage energy consumption.
CML	CML logic has reduced output voltage swing. Its consists of current bias transistor that should remain in saturation region to maintain the constant current.	due to this fast switching takes place at the input differential pair transistors. If the transistor is in sub- threshold region, Vgs voltages will be below the threshold voltage
Sub threshold Current Mode Logic (STCML)	This STCML technique dwindles the static dissipation and is also dwindling the average current flow. For high applications compared with the CMOS logic,	This depends on the various approximation levels within the ripple carry adders that are part of implemented filters in hardware which is fully synthesized in CMOS design as well as related to the
ADIABATIC	Adiabatic technique has been implemented which is also known as "ENERGY RECOVERY LOGIC".	ADIABATIC Logic has less power dissipation but even though it is not suitable to design faster switching circuits
Clocked Differential Cascode Adiabatic Logic (CDCAL)	CDCAL operated by two complementary sinusoidal power clock signals. CDCAL uses clocked control transistor for charging and discharging the output node adiabatically	These logic styles have single rail output that uses diode based control transistor for its adiabatic operation. Hence, they are suitable only for the low speed designs.
high-speed domino(HSD)	Further, they verified the energy per savings as well as reduction of hardware size in the filters with various method of design. accurate execution of the same filter.	This depends on the various approximation levels within the ripple carry adders that are part of implemented filters in hardware which is fully synthesized in CMOS design .
2N-2N2P Logic	The variation of ECRL Logic family is 2N-2N2P Logic the only difference is that two new cross coupled NMOS transistor added parallel to the two existing NMOS transistor.	the size of the transistor increases towards reducing the power consumption of TGL design circuit that is subject to the provided delay constraint.
Positive Feedback Adiabatic Logic (PFAL)	This circuit can be designed with the use of the cross-coupled inverters formed by MP1- MN3 and MP2-MN2 inverter structures that avoids a logic level degradation on the output nodes. The NMOS transistor act as a functional block for the saving of power.	But there is no availability of accurate device to perform these ternary or multi-valued logics. So, some new as well as trending technology is required for performing the multi valued logic. But, these are still in early stage of development.

Differential Cascode Pre-resolved Adiabatic Logic (DCPAL)	The arrangement of the transistor is in such a way that it acts as a differential amplifier and maintains the proper logic. The differential cascade functional block tree consists of NMOS transistors to form the PDN arm of the amplifier.	Because of low threshold voltage and negligible gate oxide thickness, there is considerable increase in the leakage energy consumption.

Conclusion: By the detailed analysis of various methods, the following challenges are identified. By adapting the FQR methodology, the area, power and delay will be significantly reduces as compared to standard Domino based logic. Major challenges regarding low power designs are as follows

- Power dissipation is the power dissipated as heat energy from electronic circuits. Reducing power dissipation has become an important constraint in day to day life. Many hand held devices with high end processors are developed making dissipation from those devices imperative. There are different semiconductor devices emerging but CMOS circuits have the special feature of low power dissipation and high noise immunity. The extensive unique features of CMOS have incorporated many low power designs in VLSI.
- Power saving methods reprocess the signal energies by adiabatic switching principle rather than dissipating as heat as well as auspicious in convinced applications wherever the speed can be dealt for the design of low power.
- Power gating is a technique for reducing the power consumption by switching off the supply voltage to the circuit blocks which are idle. This technique reduces static power dissipation because the block which remains idle is disconnected from the supply voltage. The architecture gets affected more than clock gating.
- Slew Rate needs to be maintained perfectly to avoid conflicts in data triggering. Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed as volts per second. Non linear effects in electronic amplifiers arise due to the limitations in slew rate capability. Slew rate is an important factor in the calculation of power gating efficiency. Efficiency is affected when slew rate is large.
- Switching capacitance should be stabilized, If the circuit switches at a faster rate, it affects power gating efficiency. Hence the switching capacitance change should be taken into consideration.
- Leakages of Power gate, Active transistors are used for designing power gating circuits. Hence this parameter requires reduction to ensure better working of power gating circuits and considering the high leakage in active transistors.
- Semantic gap the hardware description languages adhere to a simple, sequential programming style, which mimics the HLL programming model. They are not capable of expressing the synchronous, concurrent processing nature of the hardware circuits. This problem leads to the sub-optimal design of digital systems.
- Need to focus more towards improving the power dissipation by proposing new technology specifications, such as by implementing the FQR methodology.

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